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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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2661 #6 SP
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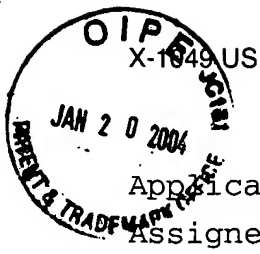
TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application / Conf. No.	10/090,519 / 6632
	Filing Date	March 01, 2002
	First Named Inventor	Paul T. Sasaki
	Examiner Name	Unassigned
	Art Unit	2661 JAN 22 2004
	Patent No.	Technology Center 2600
Mail Stop:		
Express Mail Receipt No.		
Attorney Docket Number	X-1049 US	
Total Number of Pages in This Submission		

ENCLOSURES (check all that apply)		
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<input type="checkbox"/> Amendment / Reply	<input type="checkbox"/> Declaration / Oath	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
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<input type="checkbox"/> Affidavit(s)/declaration(s)	<input type="checkbox"/> Petition -	<input checked="" type="checkbox"/> Return Receipt Postcard
<input type="checkbox"/> Extension of Time Request	<input type="checkbox"/> To Convert a Provisional Application	<input checked="" type="checkbox"/> Other Enclosure(s) (please identify below):
<input type="checkbox"/> Change Status to LARGE ENTITY	<input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address	One Copy Each of the One Hundred Four (104) References Cited
<input type="checkbox"/> Express Abandonment Request	<input type="checkbox"/> Terminal Disclaimer	
<input checked="" type="checkbox"/> Information Disclosure Statement (Supplemental)	<input type="checkbox"/> Request for Refund	
<input checked="" type="checkbox"/> Substitute PTO-1449(s) IDS by Applicant (PTO/SB/08A)		
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<input type="checkbox"/> Response to Missing Parts/Incomplete Application		
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53		
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm or Customer Number	24309 (Customer Number)	Reg. Number 51,959
Attn: Justin Liu		
Signature		
Date	January 16, 2004	Charge any additional fees required/credit any overpayment to our Deposit Account Number: 24-0040

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PATENT

IN THE UNITED STATES PATENT OFFICE

Applicants: Paul T. Sasaki et al.
Assignee: Xilinx, Inc.
Title: "Network Physical Layer with Embedded Multi-Standard CRC Generator"

Serial No.: 10/090,519 File Date: March 1, 2002
Examiner: Unknown Art Unit: 2661
Docket No.: X-1049 US Conf. No.: 6632

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Technology Center 2600

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the One Hundred Four (104) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

These references were cited in related U.S. patent applications. This Information Disclosure Statement is being filed under 37 CFR 1.97(b) prior to the receipt of a first office action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,

Justin Liu
Attorney for Applicants
Reg. No. 51,959

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Julie Matthews
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Applicati n / C nf. No.	10/090,519 / 6632
Filing Dat	March 01, 2002
First Nam d Invent r	Paul T. Sasaki
Art Unit	2661
Examiner Name	Unknown
Attorney Docket Number	X-1049 US

(use as many sheets as necessary)

Sheet	1	of	7
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Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 4,758,985	07-19-88	Carter	
		US- 5,142,625	08-25-92	Nakai	
		US- 4,855,669	08-08-89	Mahoney	
		US- 34,363	08-31-93	Freeman	
		US- 5,072,418	12-10-91	Boutaud et al.	
		US- 5,274,570	12-28-93	Izumi et al.	
		US- 5,550,782	08-27-96	Cliff et al.	
		US- 5,347,181	09-13-94	Ashby et al.	
		US- 5,339,262	08-16-94	Rostoker et al.	
		US- 6,467,009	10-15-02	Winegarden et al.	
		US- 5,914,616	06-22-99	Young et al.	
		US- 5,552,722	09-03-96	Kean	
		US- 6,578,174	06-10-03	Zizzo	
		US- 6,483,342	11-19-02	Britton et al.	
		US- 5,457,410	10-10-95	Ting	
		US- 5,740,404	04-14-98	Baji	
		US- 5,581,745	12-03-96	Muraoka	
		US- 5,742,179	04-21-98	Sasaki	
		US- 5,600,845	02-04-97	Gilson	
		US- 5,574,930	11-12-96	Halverson Jr., et al.	

[illegible]Date
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¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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		Applicati n / C nf. No.	10/090,519 / 6432		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Filing Dat	March 01, 2002		
		First Nam d Inv ntor	Paul T. Sasaki		
		Art Unit	2661		
		Examiner Name	Unknown		
		Attorney Docket Number	X-1049 US		
Sheet	2	of	7	Technology Center 2600	

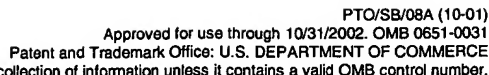
OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINL, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		IACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		P.C. FRENCH et al., "A SELF-RECONFIGURING PROCESSOR," IEEE, July 1993, pp. 50-59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		Christian Iseli et al., "SPYDER: A RECONFIGURABLE VLIW PROCESSOR USING FPGA's," IEEE, July 1993, pp. 17-24, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		MICHAEL J. WIRTHLIN et al., "THE NANO PROCESSOR: A LOW RESOURCE RECONFIGURABLE PROCESSOR," IEEE, February 1994, pp. 23-30, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		ANDRE' DEHON, "DPGA-COUPLED MICROPROCESSORS: COMMODITY ICs FOR THE EARLY 21ST CENTURY," IEEE, February 1994, pp. 31 - 39, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

Examiner Signature	Date Considered
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¹ Applicant's unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.

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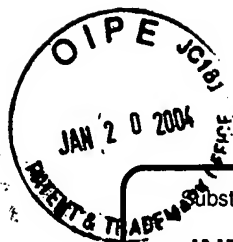
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Substitute for form 1449A/PTO		Complete if Known			
		Applicant / Conf. No.	10/090,519 / 6632		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Filing Date	March 01, 2002		
		First Named Inventor	Paul T. Sasaki		
		Art Unit	2661		
		Examiner Name	Unknown		
Sheet	4	of	7	Attorney Docket Number	X-1049 US

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OTHER -- NON PATENT LITERATURE DOCUMENTS				Technology Center 2600
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.		
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.		
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-9 to 2-18; 2-187 to 2-199, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.		
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-107 to 2-108, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.		
		CHRISTIAN ISELI et al., "AC++ COMPILER FOR FPGA CUSTOM EXECUTION UNITS SYNTHESIS," 1995, pp. 173-179, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997		
		INTERNATIONAL BUSINESS MACHINES, "POWERPC 405 EMBEDDED PROCESSOR CORE USER MANUAL," 1996, 5TH Ed., pp. 1-1 TO X-16, International Business Machines, 1580 Rout 52, Bldg. 504, Hopewell Junction, NY 12533-6531.		
		YAMIN LI et al., "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997		
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		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124		
		WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997		
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124		

Examiner Signature		Date Considered	
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Sheet	5	of	7
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Complete if Known

Applicati n / C nf. No.	10/090,519	/	6632
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Filing Date	March 01, 2002
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First Name of Inventor	Paul T. Sasaki
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Art Unit	2661
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Examiner Name	Unknown
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Attorney Docket Number	X-1049 US
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U.S. PATENT DOCUMENTS					
Examiner Initials *	Cite No.¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 6,011,407	01-04-00	New	
		US- 09/991,410	11-16-01	Herron et al.	
		US- 09/968,446	11-16-01	Herron et al.	
		US- 5,760,607	06-02-98	Leeds et al.	
		US- 5,892,961	04-06-99	Trimberger	
		US- 2003/0062922	04-03-03	Douglass et al.	
		US- 6,510,548	01-21-03	Squires	
		US- 09/917,304	07-27-01	Douglass et al.	
		US- 6,178,541	01-23-01	Joly et al.	
		US- 6,601,227	07-29-03	Trimberger	
		US- 2001/0049813	12-06-01	Chan et al.	
		US- 5,914,902	06-22-99	Lawrence et al.	
		US- 09/861,112	05-18-01	Dao et al.	
		US- 6,154,051	11-28-00	Nguyen et al.	
		US- 6,181,163	01-30-01	Agrawal et al.	
		US- 6,356,987	03-12-02	Aulas	
		US- 6,301,696	10-09-01	Lien et al.	
		US- 6,211,697	04-03-01	Lien et al.	
		US- 6,163,166	12-19-00	Bielby et al.	
		US- 6,272,451	08-07-01	Mason et al.	

[illegible]Date
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¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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		Art Unit	2661
		Examiner Name	Unknown
		Attorney Docket Number	X-1049 US
Sheet	6	of	7

OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch 3, pp 3-7 TO 3-17; 3-76 TO 3-87, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		INTERNATIONAL BUSINESS MACHINES, "PROCESSOR LOCAL BUS" Architecture Specifications, 32-Bit Implementation, April 2000, First Edition, V2.9, pp. 1-76, IBM Corporation, Department H83A, P.O. Box 12195, Research Triangle Park, NC 27709	
		XILINX, INC., "VIRTEX II PLATFORM FPGA HANDBOOK, December 6, 2000, v1.1, pp 33-75, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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Sheet	7	of	7
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Application / C nf. N .	10/090,519	/	6632
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Filing Date	March 01, 2002
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First Named Inventor	Paul T. Sasaki
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Art Unit	2661
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Examiner Name	Unknown
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Attorney Docket Number	X-1049 US
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